frequency of the ring oscillator 12 is PLL-controlled such that it coincident with a frequency of the external clock signal CLK.

5.10.07
3.5.07

On page ~~16~~ 17, at line ~~1~~ 29, please amend the paragraph as follows:

The synthesizing ratio 1:4 is selected under assumption that the voltage for regulating the characteristics of the inverters 13a of the delay line 13 is about 20% of the voltage ~~VS~~ V_s of the power source line 14 of the ring oscillator 12 as a reference.